VHiSSI Publishable Summary for 1st Reporting Period

Space-based Earth observation and scientific instrumentation currently under development will push the limits of on-board data-handling technology. In the past Mil-Std 1553 and proprietary data-links were used to get instrument data from the instruments to the on-board mass memory unit and to the down-link telemetry system. Over the past decade the proprietary data links have been replaced with a standard networking technology designed for use on-board spacecraft: SpaceWire. While SpaceWire is currently being used to fulfil the on-board data-handling requirements of many missions, there are some very high data-rate instruments which are beyond its capabilities.

Several future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers will be capable of producing data at data rates of several Gbits/s. New downlink telemetry techniques (laser and Ka-band communications) will be able to provide much higher downlink capacity than previously possible. High speed memory technologies will be able to serve multiple high data rate instruments and stream data to ground on demand. To support the growing need for onboard communications network bandwidth, technologies able to support multi-Gbits/s data transfer have been developed, e.g. Channel Link and, Wizard Link. Unfortunately these are all restricted USA devices resulting in a critical European dependency.

ESA has been developing a standard multi-Gbits/s network technology called SpaceFibre. At present this important technology is dependent upon the USA for the radiation-tolerant physical layer devices. The VHiSSI project will integrate a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. Not only will this alleviate the dependency on very high-speed serial interface devices, it will provide a complete SpaceFibre solution in a single chip, and develop an essential European radiation-tolerant ASIC fabrication capability.

The VHiSSI research programme aims to create very high-speed data-interface technology which is a critical component technology for future spacecraft payloads, particularly telecommunications and Earth observation payloads where multi-Gbits/s data-rates are urgently needed. A complete solution to very high-speed data networking onboard spacecraft will be provided, levering research on SpaceFibre, using a European fabrication facility, and providing a non-dependent technology.

The VHiSSI research programme will:

- Provide multi-Gbit/s serial data-link technology, essential for future spacecraft onboard data-handling systems.
- Lever prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provide a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provide the critical clock-recovery mechanism on existing European chip technology.
- Use a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library.
- Provide a non-dependent technology allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 284389

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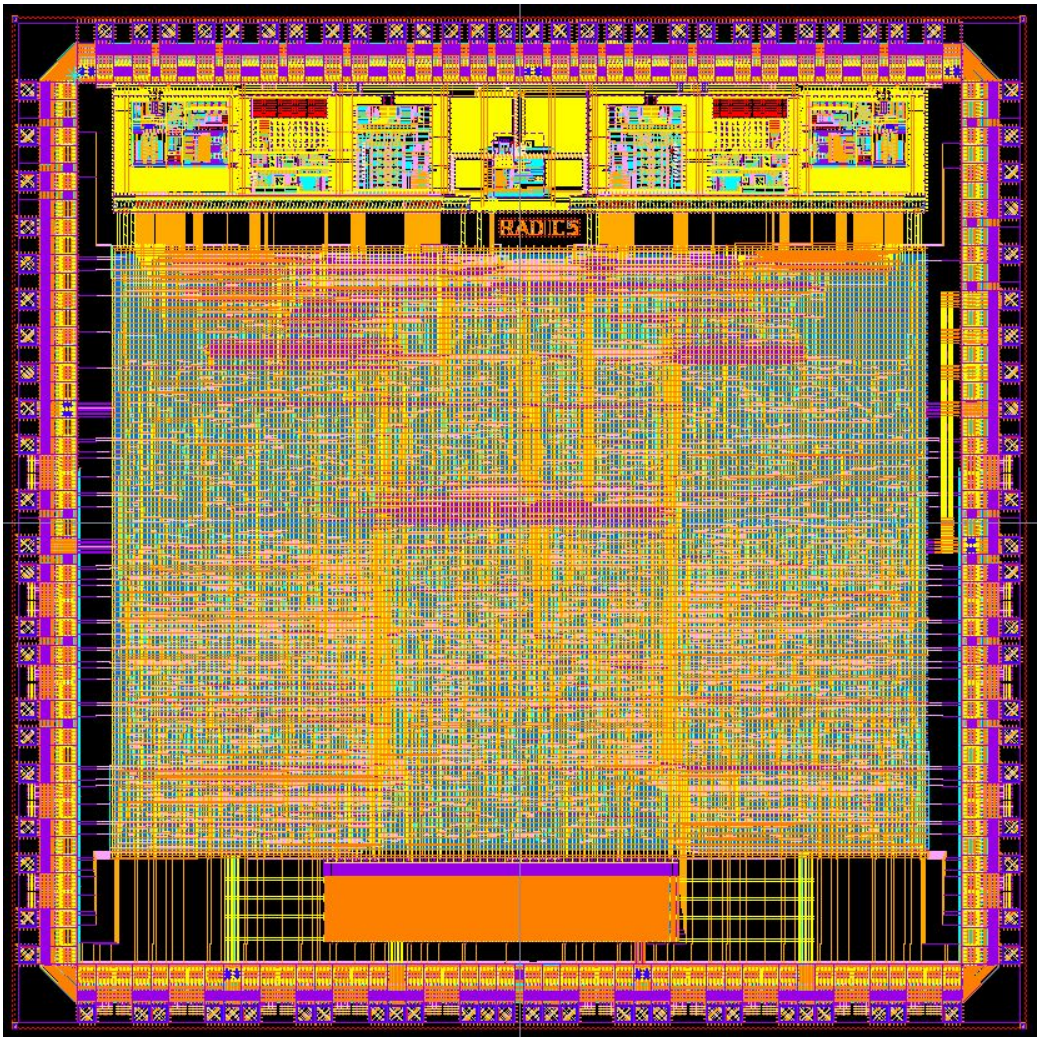
A comprehensive set of requirements for the experimental VHiSSI chip have been gathered from the European spacecraft engineering community by Astrium GmbH, focusing on a small device which could be used to provide very high-speed data-links on-board a spacecraft. A versatile chip interface has been designed by University of Dundee which covers many potential applications while keeping the number of pins required on the chip to a minimum. The architectural level design of the experimental VHiSSI chip and its interface definition have been shaped, reviewed and polished and detailed design of this chip is currently underway by STAR-Dundee Ltd.

A critical part of the VHiSSI project is the serialiser/deserialiser, clock-data recovery circuitry and the high-speed serial driver/receiver technology. This is a demanding design activity due to the speed of the interface and the required radiation tolerance. A design has been created by ACE-IC ready for testing.

The use of the IHP chip foundry required a complete radiation tolerant component library to be designed. This has been carried out by Ramon Chips and includes logic gates, IO, LVDS IO, and memory cells. A test chip has been designed and implemented which includes the critical circuitry designed by ACE-IC and library test components from Ramon Chips. This test chip is currently under test by Synergie-CAD and IHP. The results of this testing will feed into updated component design by ACE-IC and Ramon Chips which will be incorporated into the experimental VHiSSI chip.



SpaceFibre-HSSI Test Chip Layout

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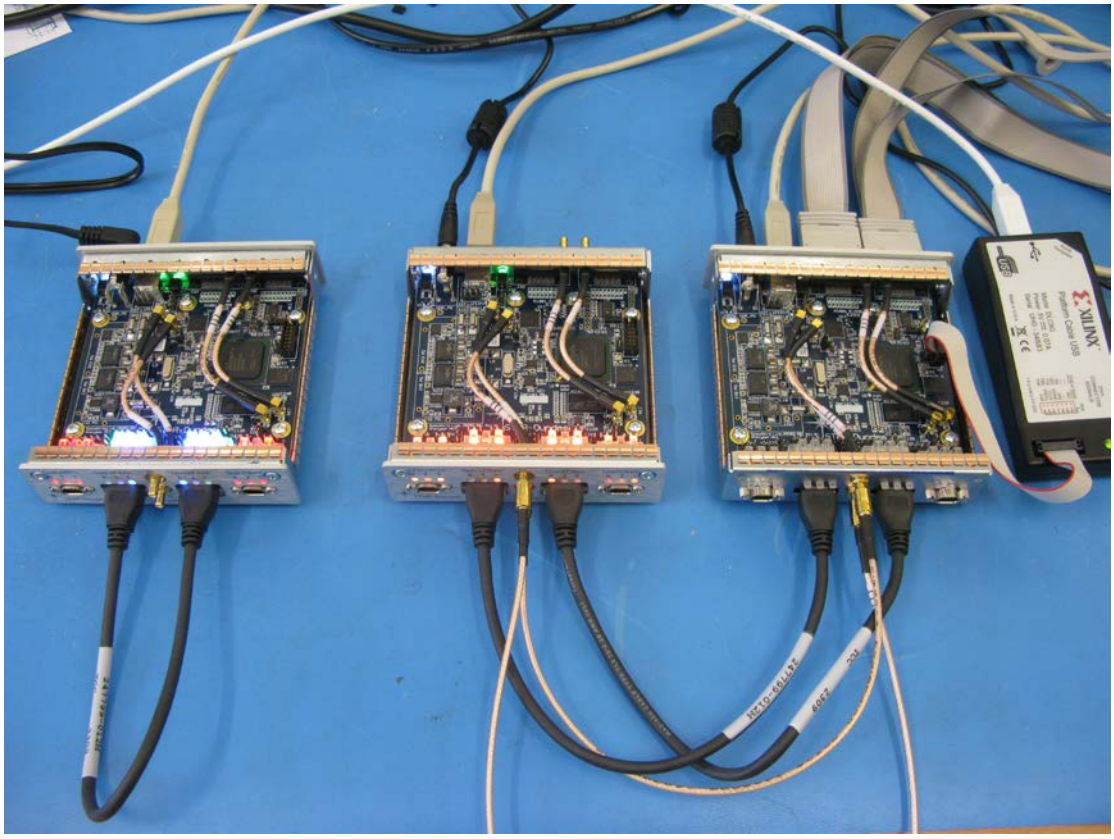
The next steps are to complete testing of the test chip, to finalise the design of the experimental VHiSSI chip, to manufacture this chip, and to test it.



Testing the VHiSSI SpaceFibre and SpaceWire Interfaces

The impact of the VHiSSI research will be very high-speed network technology for future telecommunications and Earth observation spacecraft, with terrestrial avionics, robotics, automobiles and other applications also expected to benefit.

The principal benefits of the VHiSSI research programme will be:

- Very high-speed serial-interface technology applicable to many space missions, including large and small satellites, robotic missions, planetary landers and rovers, launchers and related EGSE, and which is capable of spin-out to a wide range of terrestrial applications, including demanding robotics applications.
- Reliable and radiation-tolerant, high-speed serial interface chip implemented using a radiation-hard standard cell library optimized for a mature 130 nm CMOS process.
- Mixed-signal high-speed radiation-hardened integrated circuits that are free from international export restrictions (non-dependent) that are fabricated and tested in Europe, and that are available to members of the European Union for use in space missions.

The medium term impact of the VHiSSI programme will be an independent European technology for spacecraft high-speed data-links and network technology. The VHiSSI research will lead to a complete spacecraft onboard data-handling solution, saving mass and power, improving reliability, and substantially simplifying complex system design. This will provide a substantial European export opportunity to countries across the world.

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VHiSSI Publishable Summary for 1st Reporting Period

PROJECT DETAILS

Title	**VHiSSI: Very High Speed Serial Interfaces** (GA no. 284389)
Coordinator	**Prof Steve Parkes,** **The University of Dundee**, United Kingdom
Consortium	**STAR-Dundee Limited,** United Kingdom **RAMON chips Ltd**, Israel **ACE-IC Limited**, Israel **IHP GmbH**, Germany **Astrium GmbH**, Germany **SYNERGIE CAD INSTRUMENTS s.r.l**, Italy
Duration	1 January 2012 – 31 October 2014 (34 months)
Funding Scheme	FP7 SPACE-2011-1, topic SPA.2011.2.2-02: Space critical technologies
Budget	EU contribution: 1,999,998.98 €
Website	http://www.vhissi.eu/
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