VHiSSI Publishable Summary for 2nd Reporting Period

VHiSSI is an experimental high speed serial interface chip designed to support spaceflight applications. It implements the emerging ESA SpaceFibre standard serial communications protocol and includes important quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities.

Several important future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers will be capable of producing data at data rates of several Gbits/s. New downlink telemetry techniques (laser and Ka-band communications) will be able to provide much higher downlink capacity than previously possible. High-speed memory technologies will be able to serve multiple high data-rate instruments and stream data to ground on demand. To support the growing need for onboard communications network bandwidth, technologies able to support multi-Gbits/s data transfer have been developed, e.g. Channel Link and, Wizard Link. Unfortunately these are all restricted USA devices resulting in a critical European dependency.

SpaceFibre is a spacecraft onboard data-link and network technology being developed by University of Dundee for the European Space Agency (ESA) which runs over both copper and fibre optic cables. Initially targeted at very high data rate instruments like Synthetic Aperture Radar (SAR) and multi-spectral imaging instruments, SpaceFibre is capable of fulfilling a wider set of spacecraft onboard communications applications because of its inbuilt QoS and FDIR capabilities and its backwards compatibility with the ubiquitous SpaceWire technology.

SpaceFibre operates at 2.5 Gbits/s providing 12 times the throughput of a SpaceWire link with current flight qualified technology and allowing data from multiple SpaceWire devices to be concentrated over a single SpaceFibre link. This substantially reduces cable harness mass and simplifies redundancy strategies. The innovative QoS mechanism in SpaceFibre provides concurrent bandwidth reservation, priority and scheduled QoS. This simplifies spacecraft system engineering through integrated quality of service (QoS), which reduces system engineering costs and streamlines integration and test. Novel integrated FDIR support provides galvanic isolation, transparent recovery from transient errors, error containment in virtual channels and frames and “Babbling Idiot” protection. SpaceFibre enhances onboard network robustness through its inherent FDIR and graceful degradation techniques incorporated in the network hardware. This simplifies system FDIR software, reducing development and system validation time and cost. SpaceFibre includes low latency event signalling and time distribution with broadcast messages enabling a single network to be used for very high data rate payload data, carrying SpaceWire traffic, deterministic information for command/control, time distribution and event signalling.

SpaceFibre is backwards compatible with existing SpaceWire equipment at the packet level allowing simple interconnection of SpaceWire devices into a SpaceFibre network and enabling that equipment to take advantage of the QoS and FDIR capabilities of SpaceFibre.

Present implementations of SpaceFibre using separate SerDes and FPGA devices are dependent on USA components. The VHiSSI project has integrated a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. Not only does this alleviate the dependency on very high-speed serial interface devices, it provides a complete SpaceFibre solution in a single chip. In the process of developing the VHiSSI chip an important European radiation-tolerant ASIC fabrication capability has been demonstrated.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 284389

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The VHiSSI research programme has created a very high-speed data-interface technology which is a critical component technology for future spacecraft payloads, particularly telecommunications and Earth observation payloads where multi-Gbits/s data-rates are urgently needed. A complete solution to very high-speed data networking onboard spacecraft has been provided, levering research on SpaceFibre, using a European fabrication facility, and providing a non-dependent technology. An experimental SpaceFibre interface device (VHiSSI) has been designed to connect instrument electronics and other spacecraft equipment to SpaceFibre and also to bridge between SpaceFibre and several SpaceWire devices.

The digital logic for VHiSSI was designed by STAR-Dundee Ltd. with system architectural design and project management being carried out by University of Dundee. Airbus DS GmbH (formerly Astrium GmbH) provided inputs to the VHiSSI requirements. The design was based on RadSafeTM libraries, developed by Ramon Chips, and ported to the IHP 0.13u process. It utilizes several Radiation Hardening By Design (RHBD) techniques, which provides high immunity to all radiation effects. The libraries included standard cells, IO cells including LVDS buffers, and SRAMs with complementary EDAC logic for enhanced soft error protection. The SerDes core, which was designed by ACE-IC, was based on guidelines provided by Ramon Chips for hardening against radiation effects. Test vectors were prepared by STAR-Dundee Ltd and Synergie CAD Instruments s.r.l with inputs from other partners. The chip was manufactured by IHP. Functional and performance tests were carried out by STAR-Dundee Ltd, University of Dundee and ACE-IC. Radiation testing was carried out by Airbus DS GmbH with support from IHP and STAR-Dundee Ltd. The resulting VHiSSI chip is shown in Figure 1.

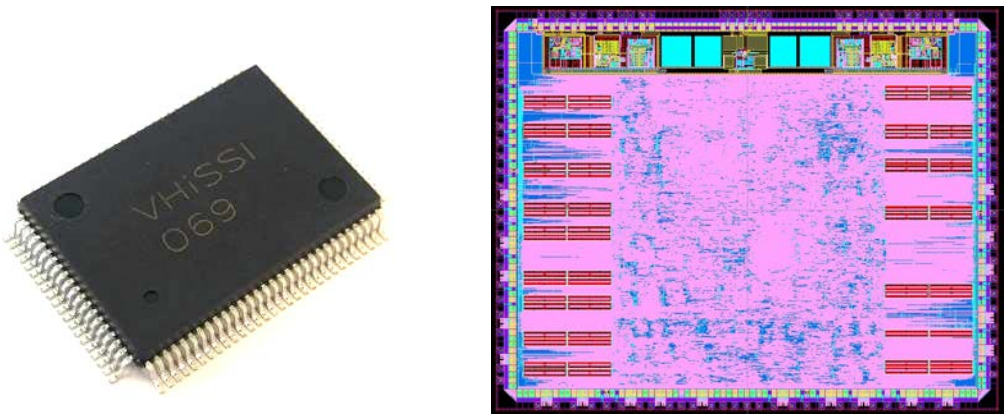

Figure 1 VHiSSI SpaceFibre Chip

A comprehensive set of requirements for the experimental VHiSSI chip were gathered from the European spacecraft engineering community by Airbus DS GmbH, focusing on a small device which could be used to provide very high-speed data-links on-board a spacecraft. A versatile chip interface was designed by University of Dundee which covers many potential applications while keeping the number of pins required on the chip to a minimum. The architectural level design of the experimental VHiSSI chip and its interface definition were shaped, reviewed and polished and detailed design of this chip carried out by STAR-Dundee Ltd.

A critical part of the VHiSSI project is the serialiser/deserialiser, clock-data recovery circuitry and the high-speed serial driver/receiver technology (SerDes). This is a demanding design activity due to the speed of the interface and the required radiation tolerance. A design was created by ACE-IC which was tested in a test chip (RADIC 5) and various improvements made for the VHiSSI chip.

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The use of the IHP chip foundry required a complete radiation tolerant component library to be designed. This was carried out by Ramon Chips and includes logic gates, IO, LVDS IO, and memory cells. The library test components from Ramon Chips were implemented in the RADIC 5 test chip and validated. Some small improvements were made to the library for the VHiSSI device.

The VHiSSI chip logic design from STAR-Dundee Ltd and the improved SerDes from ACE-IC was designed into the IHP chip technology by Ramon Chips including floor planning, place and route, and timing extraction. STAR-Dundee Ltd supported this activity carrying out static timing analysis of the placed and routed design. The chip was then manufactured by IHP on its 130 nm Bi-CMOS process.

While the chip was being manufactured Synergie CAD Instruments s.r.l, IHP and STAR-Dundee Ltd developed test vectors for chip testing and STAR-Dundee Ltd designed, implemented and tested four test boards for the VHiSSI chip covering different functions: SpaceWire LVDS, SpaceWire LVTTL, Parallel Interfaces and Radiation Testing. The VHiSSI chip was encapsulated into a plastic package and initial chip testing carried out on a chip tester at IHP. The chips that passed these tests were then used by STAR-Dundee Ltd, University of Dundee and ACE-IC for the functional and performance testing (see Figure 2).

The VHiSSI chip test results demonstrated that all functions of the chip operate as designed. The SpaceFibre interfaces operate at 2.5 Gbits/s and the SpaceWire LVDS interfaces and LVTTL interfaces operate at 200 Mbits/s. The VHiSSI SpaceWire LVDS test board operated successfully with a STAR Fire SpaceFibre interface and link analyser device, and also with another VHiSSI device. The eye diagram of the SerDes is shown in Figure 3. Radiation testing was carried out by Airbus DS GmbH, IHP and STAR-Dundee Ltd. Both total ionising dose (TID) testing and single event effect (SEE) testing have been carried out. While the TID test results were excellent, there was a problem with the SEE testing which requires further investigation.

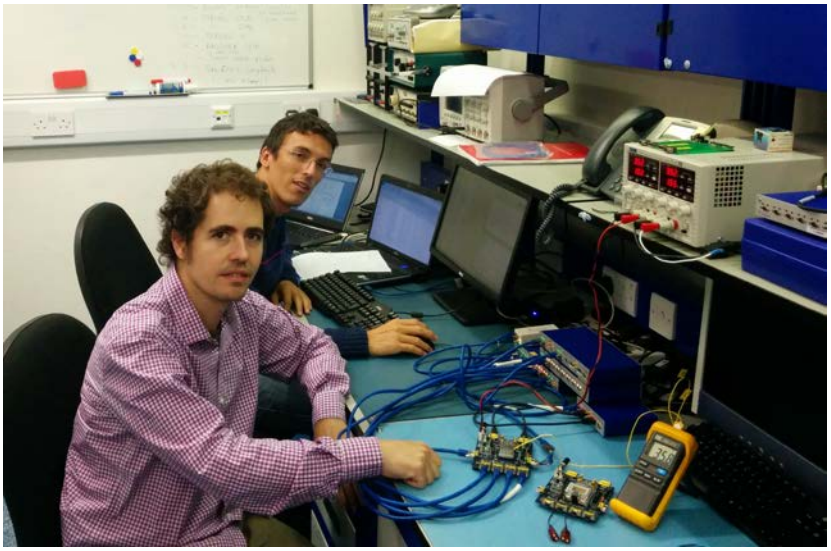

Figure 2 Testing the VHiSSI SpaceFibre and SpaceWire Interfaces

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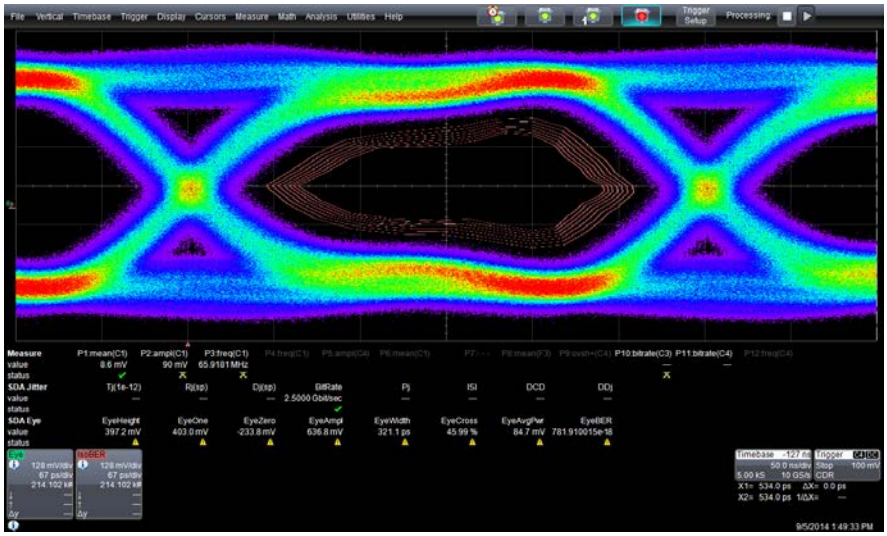

Figure 3 VHiSSI Transmit Eye Pattern at 2.5 Gbits/s

The VHiSSI research programme has researched, designed and developed an experimental high speed serial interface device, VHiSSI, which:

- Provides multi-Gbit/s serial data-link technology, essential for future spacecraft onboard data-handling systems.
- Levers prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provides a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provides the critical clock-recovery mechanism on existing European chip technology.
- Uses a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library. Further work needs to be done related to the SEE testing.
- Provides a non-dependent technology allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

The impact of the VHiSSI research is a very high-speed network technology for future telecommunications and Earth observation spacecraft, with terrestrial avionics, robotics, automobiles and other applications also expected to benefit.

The principal benefits of the VHiSSI research programme are:

- Very high-speed serial-interface technology applicable to many space missions, including large and small satellites, robotic missions, planetary landers and rovers, launchers and related EGSE, and which is capable of spin-out to a wide range of terrestrial applications, including demanding robotics applications.
- A high-speed serial interface chip implemented using a radiation-hard standard cell library optimized for a new 130 nm CMOS process, although further work needs to be carried out related to SEE.
- Mixed-signal high-speed radiation-hardened integrated circuits that are free from international export restrictions (non-dependent) that are fabricated and tested in Europe, and that are available to members of the European Union for use in space

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missions. The SEE issue detected in the last month of the project needs to be addressed.

The medium term impact of the VHiSSI programme will be an independent European technology for spacecraft high-speed data-links and network technology. The VHiSSI research will lead to a complete spacecraft onboard data-handling solution, saving mass and power, improving reliability, and substantially simplifying complex system design. This will provide a substantial European export opportunity to countries across the world.

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PROJECT DETAILS

Title	**VHiSSI: Very High Speed Serial Interfaces** (GA no. 284389)
Coordinator	**Prof Steve Parkes,** **The University of Dundee,** United Kingdom
Consortium	**STAR-Dundee Limited,** United Kingdom **RAMON chips Ltd**, Israel **ACE-IC Limited,** Israel **IHP**, Germany **Airbus DS GmbH**, Germany **SYNERGIE CAD INSTRUMENTS s.r.l**, Italy
Duration	1 January 2012 – 31 October 2014 (34 months)
Funding Scheme	FP7 SPACE-2011-1, topic SPA.2011.2.2-02: Space critical technologies
Budget	EU contribution: 1,999,998.98 €
Website	http://www.vhissi.eu/
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